Welcome to the 26th Asian Test Symposium (ATS’17)! Since its debut in 1992, Asian Test Symposium has been the largest event in Asia that focuses on the testing of integrated circuits and systems, and has attracted researchers and engineers from all over the world to share their experiences and knowledge. In 2017, the symposium comes to Taipei—the capital of Taiwan.

The technical program of ATS’17 responds to many challenges in the integrated circuits and systems design and manufacturing industries. In addition to research papers and presentations, two special sessions covering the topics of “emerging memory test and reliability” and “hardware-oriented security and trust” will be given. The topics of research papers cover the scope of memory test and reliability, design debug and verification, yield enhancement, diagnosis, scan test, hardware security, etc. In addition to the technical and special sessions, ATS’17 features three keynote speeches and one invited talk will be given by the speakers, Prof. Hans-Joachim Wunderlich from Universität Stuttgart, Dr. Yervant Zorian from Synopsys, Dr. Wu-Tung Cheng from Mentor Graphics, and Dr. Shih-Lien Lu from TSMC. The ATS’17 also will have two half-day tutorials given by Prof. Wen (Kyushu Institute of Technology), Prof. Girard (LIRMM / CNRS), and Prof. Chakrabarty (Duke University) cover the power-aware testing and data-driven resiliency solutions. Finally, ATS’17 also hosts the semi-final competition of E. J. McCluskey Doctoral Thesis Award.

We hope that you will enjoy the fruitful program of ATS’17. On behalf of the steering committee and organizing committee of ATS’17, we sincerely thank you for the participation and hope that you will keep making ATS a success by actively participating in it.

Welcome to Taipei and enjoy ATS’17!

General Chair
Jiun-Lang Huang, National Taiwan University
Program Chair
Jin-Fu Li, National Central University
Organizing Committee

General Chair
Jiun-Lang Huang, National Taiwan Univ.

Program Chair
Jin-Fu Li, National Central Univ.

Tutorial Chair
Katherine Shu-Min Li, National Sun Yat-Sen Univ.

Publicity Chair
Shi-Yu Huang, National Tsing Hua Univ.

Publication Chair
Pi-Ho Hu, National Central Univ.

Finance Chair
Chin-Ya Huang, National Central Univ.

Local Arrangement Chair
Tong-Yu Hsieh, National Sun Yan-Set Univ.

Registration Chair
Shuye-Kung Lu, National Taiwan Univ. of Science and Tech.

Industry Chair
Chun-Lung Hsu, Industrial Technology Research Institute

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Yiorgos Makris, Texas at Dallas Univ.

European Liaison
Said Hamdioui, Delft of Technology Univ.
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Krishnendu Chakrabarty, Duke Univ.
Patrick Girard, LIRMM / CNRS
Masaki Hashizume, Univ. of Tokushima
Shi-Yu Huang, National Tsing Hua Univ.
Jinn-Lang Huang, National Taiwan Univ.
Tomoo Inoue, Hiroshima City Univ.
Seiji Kajihara, Kyushu Institute of Technology
Kuen-Jong Lee, National Cheng Kung Univ.
Huawei Li, Chinese Academy of Sciences
Xiaowei Li, Chinese Academy of Sciences
Virendra Singh, Indian Institute of Science
Hiroshi Takahashi, Ehime Univ.
Sying-Jyan Wang, National Chung Hsing Univ.
Shiyi Xu, Shanghai Univ.
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Lorena Anghel - Univ. Grenoble-Alpes
Bernd Becker - Albert-Ludwigs-Univ. Freiburg
Soon-Jyh Chang - National Cheng Kung Univ.
Mango Chao - National Chiao Tung Univ.
Harry Chen - MediaTek
Masahiro Fujita - Univ. of Tokyo
Patrick Girard - LIRMM
Dimitris Gizopoulos - Univ. of Athens
Xinli Gu - Huawei
Masaki Hashizume - The Univ. of Tokushima
Gurgen Harutyunyan - Synopsys
Sybille Hellbrand - Univ. of Paderborn
Hao-Chiao Hong - National Chiao Tung Univ.
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Tong-Yu Hsieh - National Sun Yat-sen Univ.
Chih-Tsun Huang - National Tsing Hua Univ.
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Naghmeh Karimi - Univ. of Maryland
Ramesh Karri - New York Univ.
Rohit Kapur - Synopsys
Michael Kochte - Univ. of Stuttgart
Erik Larsson - Lund Univ.
Kuen-Jong Lee - National Cheng Kung Univ.
Jin-Fu Li - National Central Univ.
Huawei Li - Chinese Academy of Sciences
Chien-Mo Li - National Taiwan Univ.
Katherine Shu-Min Li - National Sun Yat-sen Univ.
Xiaowei Li - Chinese Academy of Sciences
Jing-Jia Liou - National Tsing Hua Univ.
Shyue-Kung Lu - National Taiwan Univ. of Science and Technology
Erik Jan Marinissen - IMEC
Cecilia Metra - Univ. of Bologna
Satoshi Ohtake - Oita Univ.
Chia Yee Ooi - Universiti Teknologi
Alex Orailoglu - Univ. of California, San Diego
Rubin Parekhji - Texas Instruments
Irith Pomeranz - Purdue Univ.
Seetal Potluri - Xilinx Asia Pacific Pte. Ltd.
Janusz Rajski - Mentor Graphics
Sudhakar Reddy - Univ. of Iowa
Kewal Saluja - Univ. of Wisconsin-Madison
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Adit Singh - Auburn Univ.
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Mottaqiallah Taouil - Technische Universiteit Delft
Mark Tehranipoor - Univ. of Florida
Nur Touba - University of Texas at Austin
Hans Tsai - Mentor Graphics
Li-C Wang - Univ. of California, Santa Barbara
Xiaqing Wen - Kyushu Institute of Technology
Charles Hung-Pin Wen - National Chiao Tung Univ.
Cheng-Wen Wu - National Tsing Hua Univ.
Hans-Joachim Wunderlich - Universität Stuttgart
Dong Xiang - Tsinghua Univ.
Shiyi Xu - Shanghai Univ.
Qiang Xu - The Chinese Univ. of Hong Kong
Organizer
National Taiwan Univ.
National Central Univ.

Dates / Symposium Venue

<table>
<thead>
<tr>
<th>Dates</th>
<th>Nov. 27-30, 2017</th>
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</thead>
<tbody>
<tr>
<td>Venue</td>
<td>Palais de Chine Hotel (5F)</td>
</tr>
<tr>
<td></td>
<td>No. 3, Section 1, Chengde Road, Taipei 103</td>
</tr>
<tr>
<td>Phone</td>
<td>+886-2-2181-9999</td>
</tr>
<tr>
<td>Email</td>
<td><a href="mailto:palais@ldchotels.com">palais@ldchotels.com</a></td>
</tr>
<tr>
<td>Web</td>
<td><a href="http://www.palaisdechinehotel.com">http://www.palaisdechinehotel.com</a></td>
</tr>
</tbody>
</table>

Registration / Information Hours

ATS registration desk is at 5F
Monday, Nov. 27 08:00-16:30
Tuesday, Nov. 28 08:00-16:30
Wednesday, Nov. 29 08:00-12:00
Thursday, Nov. 30 08:00-10:00

Board

• The welcome reception will be 18:00 ~ 20:00, Mon., Nov. 27 at Room 402, NTUH International Convention Center.
• The social event will be 13:30 ~ 17:00, Wed., Nov. 29 at the National Palace Museum.
• The banquet will be 17:30 ~ 21:00, Wed., Nov. 29 at 12F the Kunlun Hall, Grand Hotel Taipei.
### Program at a glance

#### Nov. 27, 2017, Monday

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>09:00~10:20</td>
<td>Tutorial 1 – Power-Aware Testing in the Era of IoT</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>10:20~10:40</td>
<td>Coffee Break</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>10:40~12:00</td>
<td>Tutorial 1 – Power-Aware Testing in the Era of IoT</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>12:00~13:30</td>
<td>Lunch</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>13:30~14:50</td>
<td>Tutorial 2 – Data-Driven Resiliency Solutions for Integrated Circuits and Systems</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>14:50~15:10</td>
<td>Coffee Break</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>15:10~16:30</td>
<td>Tutorial 2 – Data-Driven Resiliency Solutions for Integrated Circuits and Systems</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>16:30~18:00</td>
<td>Coffee Break</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>18:00~20:00</td>
<td>Coffee Break</td>
<td>Grand Hall A</td>
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</tbody>
</table>

#### Nov. 28, 2017, Tuesday

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>09:00~10:30</td>
<td>Keynote 1 – The Revival of BIST: From Self-Test to Self-Healing</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>10:30~11:00</td>
<td>Coffee Break</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>11:00~11:50</td>
<td>Invited Talk – A Foundry's View of Hardware Security</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>11:50~13:00</td>
<td>Lunch</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>13:00~14:15</td>
<td>Session 1A – PhD Thesis Award Contest</td>
<td>Grand Hall A</td>
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<tr>
<td>14:15~14:45</td>
<td>Coffee Break</td>
<td>Grand Hall A</td>
</tr>
<tr>
<td>14:45~16:25</td>
<td>Session 2A – Hardware Security</td>
<td>Grand Hall A</td>
</tr>
</tbody>
</table>
## Program at a glance

**Nov. 29, 2017, Wednesday**

<table>
<thead>
<tr>
<th>Time</th>
<th>Grand Hall</th>
<th>Room</th>
<th>Program</th>
</tr>
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<tbody>
<tr>
<td>08:30~10:10</td>
<td></td>
<td></td>
<td>Keynote 2 – Addressing Automotive Safety Challenge &amp; Solutions</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Speaker: Yervant Zorian (Synopsys)</td>
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<tr>
<td>10:10~10:40</td>
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<td></td>
<td>Keynote 3 – Volume Diagnosis</td>
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<td></td>
<td></td>
<td></td>
<td>Speaker: Wu-Tung Cheng (Mentor Graphics)</td>
</tr>
<tr>
<td>10:40~12:20</td>
<td></td>
<td>Grand Hall A</td>
<td>Session 3A – Special Session on Hardware-Oriented Security and Trust</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Lunch (GSC Hiroshima High School Research Poster Presentation)</td>
</tr>
<tr>
<td>12:20~13:30</td>
<td></td>
<td>Grand Hall B</td>
<td>Session 3B – Scan Test</td>
</tr>
<tr>
<td>13:30~17:00</td>
<td></td>
<td></td>
<td>Social Event</td>
</tr>
<tr>
<td>17:30~21:00</td>
<td></td>
<td></td>
<td>Banquet @ Grand Hotel</td>
</tr>
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</table>

**Nov. 30, 2017, Thursday**

<table>
<thead>
<tr>
<th>Time</th>
<th>Grand Hall</th>
<th>Room</th>
<th>Program</th>
</tr>
</thead>
<tbody>
<tr>
<td>08:30~09:45</td>
<td></td>
<td>Grand Hall A</td>
<td>Session 4A – Special Session on Test and Reliability of Emerging Memories</td>
</tr>
<tr>
<td>09:45~10:15</td>
<td></td>
<td>Grand Hall B</td>
<td>Session 4B – Debugging and Design</td>
</tr>
<tr>
<td>10:15~11:30</td>
<td></td>
<td></td>
<td>Session 5A – Advanced Diagnosis Techniques</td>
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<td></td>
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<td></td>
<td>Session 5B – Design for Testability</td>
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<tr>
<td></td>
<td></td>
<td>Room Descartes &amp; Rousseau</td>
<td>Session 3C – Advanced Testing Techniques</td>
</tr>
</tbody>
</table>
08:00 – 09:00 Registration
09:00 – 12:00 Tutorial #1 (Grand Hall A)

Power-Aware Testing in the Era of IoT
Presenter #1: Xiaoqing Wen (Kyushu Institute of Technology)
Presenter #2: Patrick Girard (LIRMM / CNRS)

12:00 – 13:30 Lunch

13:30 – 16:30 Tutorial #2 (Grand Hall A)

Data-Driven Resiliency Solutions for Integrated Circuits and Systems
Presenter: Krishnendu Chakrabarty (Duke Univ.)

18:00 – 20:00 Reception (Room 402)

Venue: Room 402, NTUH International Convention Center
Address: Room 402, 4F, No.2, Xuzhou Rd., Zhongzheng Dist., Taipei City 100, Taiwan (R.O.C.).

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PNSyn: Power Delivery Network Synthesis
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08:00 – 09:00 Registration

09:00 – 10:30 Plenary Session (Grand Hall)

Welcome Message
Jiun-Lang Huang (National Taiwan Univ.), General Chair

Program Introduction
Jin-Fu Li (National Central Univ.), Program Chair

Keynote #1: The Revival of BIST: From Self-Test to Self-Healing
Chair: Kuen-Jong Lee (National Cheng Kong Univ.)
Presenter: Hans-Joachim Wunderlich (University of Stuttgart)

10:30 – 11:00 Break

Invited Talk: A Foundry’s View of Hardware Security
Chair: Jiun-Lang Huang (National Taiwan Univ.)
Presenter: Shih-Lien Lu (TSMC)

11:50 – 13:00 Lunch (Grand Hall)

13:00 – 14:15 Session 1A (Grand Hall A)

PhD Thesis Award Contest
Organizer & Moderator: Hiroshi Takahashi, Ehime Univ.

- Trace based design for debug for Post-silicon Validation
  Yun Cheng and Huawei Li (Chinese Academy of Science)

- Testing and Synthesis of Reversible Logic Circuit
  Bikromadittya Mondal and Susanta Chakraborty (Indian Institute of Engineering Science and Technology)

- Field Test for Ensuring the Functional Safety of Automotive System
  Hanan T. Al-Awadhi and Hiroshi Takahashi (Ehime Univ.)

- Power Side-channel Analysis Based Hardware Trojan Detection through Circuit Partitioning
  Fakir Sharif Hossain and Michiko Inoue (NAIST)
  Alex Orailoglu (UCSD)
13:00 – 14:15 Session 1B (Grand Hall B)

**Interconnect Test and Measurement**
Moderator: Shu-Min Li (National Sun Yat-sen Univ.)

- **An enhanced boundary scan architecture for inter-die interconnect leakage measurement in 2.5D and 3D packages**
Pok Man Law and Cheng-Wen Wu (National Tsing Hua Univ.)
Hao-Chiao Hong and Long-Yi Lin (National Chiao Tung Univ.)

- **On-chip ring oscillator based scheme for TSV delay measurement**
Songwei Pei and Alrashdi Ahmed Rabehb (Beijing Univ. of Chemical Technology)
Song Jin (North China Electric Power Univ.)

- **Testing of interconnect defects in memory based reconfigurable logic device (MRLD)**
Senling Wang, Yoshinobu Higami, and Hiroshi Takahashi (Ehime Univ.)
Masayuki Sato and Mitsunori Katsu (TRL Corp.)
Shoichi Sekiguchi (Taiyo Yuden)

13:00 – 14:15 Session 1C (Descartes & Rousseau)

**Test Compression**
Moderator: Chun-Lung Hsu (ITRI)

- **Test pattern compression for probabilistic circuits**
Chih-Ming Chang, Kai-Chieh Yang, James Chien-Mo Li and Hung Chen (National Taiwan Univ.)

- **Test compression with single-input data spreader and multiple test sessions**
Chang-Wen Chen, Yi-Cheng Kong and Kuen-Jong Lee (National Cheng Kong Univ.)

- **Test compaction with dynamic updating of faults for coverage of undetected transition faults sites**
Irith Pomeranz (Purdue Univ.)

14:15 – 14:45 Break
14:45 – 16:25 Session 2A (Grand Hall A)

**Hardware Security**
Moderator: Sying-Jyan Wang (National Chung Hsing Univ.)

- **A new active IC metering technique based on locking scan cells**
  Aijiao Cui, and Xuesen Qian (Harbin Institute of Technology Shenzhen Graduate School)
  Gang Qu (Maryland Univ.)
  Huawei Li (Chinese Academy of Sciences)

- **Tree-based logic encryption for resisting SAT attack**
  Yung-Chih Chen (Yuan Ze Univ.)

- **Intra-die-variation-aware side channel analysis for hardware Trojan detection**
  Fakir Sharif Hossain, Tomokazu Yoneda, Michihiro Shintani, and Michiko Inoue (NAIST)
  Alex Orailoglu (UCSD)

- **On securing scan design from scan-based side-channel attacks**
  Satyadev Ahlawat and Darshit Vaghani (Indian Institute of Technology Bombay)
  Jaynarayan T Tudu (Indian Institute of Science)
  Virendra Singh (Indian Institute of Technology Bombay)

14:45 – 16:25 Session 2B (Grand Hall B)

- **Circuits and Systems Reliability Enhancement Techniques**
  Moderator: Aijiao Cui (Harbin Institute of Technology Shenzhen Graduate School)

- **An incremental aging analysis method based on Delta circuit simulation technique**
  Si-Rong He, Nguyen Cao Qui, Yu-Hsuan Kuo, and Chien-Nan Liu (National Central Univ.)

- **Post-silicon test flow for aging prediction**
  Hau Hsu, Jing-Jia Liou, Zih-Huan Gao, and Ting-Shuo Hsu (National Tsing Hua Univ.)
Cloud-based PVT monitoring system for IoT devices
Guan-Hao Lian, Shi-Yu Huang, and Wei-Yi Chen (National Tsing Hua Univ.)

A critical charge model for estimating the SET and SEU sensitivity: a Muller C-element case study
Marko Andjelkovic, Milos Krstic, and Rolf Kraemer (IHP) 
Varadan Savulimedu Veeravalli and Andreas Steininger (TU Wien)

14:45 – 16:25 Session 2C (Descartes & Rousseau)

Techniques for Testing and Reliability
Moderator: Tong-Yu Hsieh (National Sun Yat-sen Univ.)

Design and Implementation of an EG-pool based FPGA formatter with temperature compensation
Yang-Kai Huang, Kuan-Te Li, Chih-Lung Hsiao, Chia-An Lee, and Jiun-Lang Huang (National Taiwan Univ.)
Terry Kuo (OpenATE)

SAR TDC architecture with self-calibration employing trigger circuit
Yuki Ozawa, Takashi Ida, Rishen Jiang, Shotaro, Sakurai, Seiya Takegami, and Nobukazu Tsukiji (Gunma Univ.)
Ryoji Shiota (Socionex)
Haruo Kobayashi (Gunma Univ.)

Bringing fault-tolerant GigaHertz-computing to space: A Multi-Stage Software-Side Fault-Tolerance Approach for Miniaturized Spacecraft
Christian M. Fuchs, Todor P. Stefanov, Nadia M. Murillo, and Aske Plaat (Leiden Univ.)

Identification of efficient clustering technique for test power activity on the layout
Harshad Dhotre, Stephan Eggersglüss, and Rolf Drechsler (Univ. of Bremen)
08:00 – 08:30 Registration
08:30 – 10:10 Keynote Session (Grand Hall)

Keynote #2: Addressing Automotive Safety Challenge & Solutions
Chair: Cheng-Wen Wu (National Tsing-Hua Univ.)
Presenter: Yervant Zorian (Synopsys)

Keynote #3: Volume Diagnosis
Chair: Shi-Yu Huang (National Tsing-Hua Univ.)
Presenter: Wu-Tung Cheng (Mentor Graphics)

10:10 – 10:40 Break
10:40 – 12:20 Session 3A (Grand Hall A)

Special Session on Hardware-Oriented Security and Trust
Organizer & Moderator: Huawei Li (Chinese Academy of Sciences)

- Securing Infrastructure IP in Today’s SoCs
  Yervant Zorian (Synopsys)

- Security Implications of Cyberphysical Flow-based Microfluidic Biochips
  Jack Tang, Ramesh Karri (New York Univ.)
  Mohamed Ibrahim, Krishnendu Chakrabarty (Duke Univ.)

- How to Secure Scan design against scan-based side-channel attacks?
  Wei Zhou, Aijiao Cui (Harbin Institute of Technology Shenzhen Graduate School)
  Huawei Li (Chinese Academy of Sciences)
  Gang Qu (University of Maryland College Park)

10:40 – 12:20 Session 3B (Grand Hall B)

Scan Test
Moderator: Chien-Mo Li (National Taiwan Univ.)

- Structure-oriented test of reconfigurable scan networks
  Dominik Ull, Kochte Michael, and Hans-Joachim Wunderlich (Univ. of Stuttgart)
- **Compaction of a transparent-scan sequence to reduce the fail data volume for scan chain faults**
  Irith Pomeranz (Purdue Univ.)

- **Architecture for reliable scan-dump in the presence of multiple asynchronous clock domains in FPGA SoCs**
  Amitava Majumdar, Balakrishna Jayadev, Da Cheng, and Albert Lin (Xilinx)

- **Scan chain grouping for mitigating IR-drop-induced test data corruption**
  Yucong Zhang, Stefan Holst, Xiaoqing Wen, Kohei Miyase, and Seiji Kajihara (Kyushu Institute of Technology)
  Jun Qian (Advanced Micro Devices)

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- Highly optimized, memory-efficient engines
- 10X Faster Runtime, 25% Fewer Patterns
- Re-use of proven interfaces enables easy, risk-free deployment
- Certified for ISO 26262 automotive functional safety
10:40 – 12:20 Session 3C (Descartes & Rousseau)

**Advanced Testing Techniques**
Moderator: Chia-Tso Chao (National Chiao Tung Univ.)

- **Deterministic path delay measurement using short cycle test pattern**
  Kentaro Kato (Tsuruoka College)

- **Cell-aware ATPG to improve defect coverage for FPGA IPs and next generation MSPSoCs**
  Seetal Potluri, Aaron Mathew, Rambabu Nerukonda, Ismed Hartanto, and Shahin Toutounchi (Xilinx)

- **Testing clock distribution networks**
  Sying-Jyan Wang, Hsiang-Hsueh Chen, and Chin-Hung Lien (National Chung-Hsing Univ.)
  Katherine Shu-Min Li (National Sun Yat-sen Univ.)

- **Test coverage analysis for designs with timing exceptions**
  Kun-Han Tsai (Mentor Graphics)
  Srinivasan Gopalakrishnan (Qualcomm)
12:20 – 13:30 Lunch (Grand Hall)
GSC Hiroshima High School Student Research Poster Presentation 2017
13:30 – 17:00 Social Event
17:30 – 21:00 Banquet (12F, Kunlun Hall)

Venue: The Grand Hotel
Address: 12F, No.1, Sec. 4, Zhongshan N. Rd., Taipei City

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Mentor Graphics Tessent product line covers everything from test definition, test bring-up, silicon characterization, water test, package test, failure diagnosis and yield analysis for IC logic, memory, analog, and I/O. Tessent includes a comprehensive set of targeted test solutions to meet ISO 26262 quality and reliability requirements. All Tessent solutions are part of the Mentor Safe program and are ISO 26262 certified for use on ASIL D designs. Visit our website at go.mentor.com/sts
08:00 – 08:30 Registration

08:30 – 09:45 Session 4A (Grand Hall A)

Special Session on Test and Reliability of Emerging Memories
Organizer & Moderator: Said Hamdioui (Delft Univ. of Technology)

- Test and Reliability of STT-MRAMs
  Arijit Raychowdhury (Georgia Institute of Technology)

- Test and Reliability of PCMs
  Huawei Li (Chinese Academy of Sciences)

- Test and Reliability of RRAMs
  Said Hamdioui (Delft Univ. of Technology)

08:30 – 09:45 Session 4B (Grand Hall B)

Debugging and Design Verification
Moderator: Seetal Potluri (Xilinx)

- Test and debug strategy for high speed JESD204B Rx PHY
  Surya Piplani, Vivek Mohan Sharma, and Daniele Cervini (STMicroelectronics)
  Humberto Fonseca and David Hardisty (Cadence Design Systems)

- Post silicon debugging of electrical bugs using trace buffers
  Kentaro Iwata and Amir Masoud Ghareshbaghi (Univ. of Tokyo)
  Mehdi Tahoori (Karlsruhe Institute of Technology)
  Masahiro Fujita (Univ. of Tokyo)

- On evaluating and constraining assertions using conflicts in absent scenarios
  Huina Chao, Huawei Li, Xiaoyu Song, Tiancheng Wang, and Xiaowei Li (Chinese Academy of Sciences)
08:30 – 09:45 Session 4C (Descartes & Rousseau)

**Yield Enhancement and Diagnosis**
Moderator: Tomoo Inoue (Hiroshima Univ.)

- **Yield enhancement by repair circuits for ultra-fine pitch stacked-chip connections**
  Keitaro Koga, Hiromitsu Awano, and Makoto Ikeda (Univ. of Tokyo)

- **Error-tolerability evaluation and test for images in face detection application**
  Tong-Yu Hsieh, Tai-Ang Cheng, and Chao-Ru Chen (National Sun Yat-sen Univ.)

- **PADLOC: physically-aware defect localization and characterization**
  Soumya Mittal and Shawn Blanton (Carnegie Mellon)

09:45 – 10:15 Break

10:15 – 11:30 Session 5A (Grand Hall A)

**Advanced Diagnosis Techniques**
Moderator: Xinli Gu (Huawei)

- **Automatic identification of yield limiting layout patterns using root cause deconvolution on volume scan diagnosis data**
  Wu-Tung Cheng, Randy Klingenberg, Brady Benware, Wu Yang, Manish Sharma, and Geir Eide (Mentor Graphics)
  Yue Tian and Sudhakar M. Reddy (Univ. of Iowa)
  Yan Pan, Sherwin Fernandes, and Atul Chittora (Global Foundaries)

- **Scan chain diagnosis based on unsupervised machine learning**
  Yu Huang, Brady Benware, Randy Klingenberg, Huaxing Tang, Jayant Dsouza, and Wu-Tung Cheng (Mentor Graphics)

- **Using cell aware diagnostic patterns to improve diagnosis resolution for cell internal defects**
  Huaxing Tang (Mentor Graphics)
  Arvind Jain, Sanil Kumark Pillai, and Dharmesh Joshi ( Qualcomm)
  Shamitha Rao (Mentor Graphics)
10:15 – 11:30 Session 5B (Grand Hall B)

**Design for Testability**

Moderator: Masayuki Arai (Nihon Univ.)

- **Automotive IC on-line test techniques and the application of deterministic ATPG-based runtime test**
  - Yoichi Maeda, Jun Matsushima (Renesas System Design)
  - Ron Press (Mentor Graphics)

- **Open defect detection with built-in test circuit by IDDT appearance time in CMOS ICs**
  - Ayumu Kambara, Hiroyuki Yotsuyanagi, Daichi Miyoshi, and Masaki Hashizume (Tokushima Univ.)
  - Shyue-Kung Lu (National Taiwan Univ. of Science and Technology)

- **Design for testability technique of reversible logic circuits based on exclusive testing**
  - Joyati Mondal and Debesh Kumar Das (Jadavpur Univ.)

10:15 – 11:30 Session 5C (Descartes & Rousseau)

**Memory Test and Reliability**

Moderator: Masahiro Fujita (Univ. of Tokyo)

- **Fault-aware page address remapping techniques for enhancing yield and reliability of flash memories**
  - Shyue-Kung Lu and Shu-Chi Yu (National Taiwan Univ. of Science and Technology)
  - Masaki Hashizume (The Univ. of Tokushima)

- **3D IC memory BIST controller allocation for test time minimization under power constraints**
  - Yen-Chun Ko and Shih-Hsu Huang (Chung Yuan Christian Univ.)

- **A heuristic algorithm for Automatic generation of march tests**
  - Xiaole Cui, Yichi Luo, and Qiujun Lin (Peking Univ. Shenzhen Graduate School)
  - Xiaoxin Cui (Peking Univ.)
Welcome Reception
Monday, Nov. 27
The welcome reception will take place on Monday, Nov. 27 at Room 402, 4F, NTUH International Convention Center from 18:00-20:00.
Address: Room 402, 4F, No.2, Xuzhou Rd., Zhongzheng Dist., Taipei City

Direction to Reception from Palais de Chine Hotel by MRT
• 1. Please get on the metro Taipei Main Station and get off at NTU Hospital Station, Exit 2.
• 2. Please get on the metro Taipei Main Station and get off Shandao Temple Station, Exit 2.
Social Program

Wednesday, Nov. 29

The social event on Wednesday, Nov. 29, will take place at the National Palace Museum followed by a banquet at the Grand Hotel. Buses will depart sharply on 13:30 from the Conference Venue. Comfortable clothing and shoes are recommended.

Social Event

13:30-17:00 - National Palace Museum

The National Palace Museum (NPM) houses a collection of ancient Chinese artifacts, some of which came from The Palace Museum and the preparatory department of the Nanjing Museum (previously the "National Central Museum"); those that came from The Palace Museum originated from the Qing Court, and those that came from the preparatory department of the Nanjing Museum primarily originated from the Institute for Exhibiting Antiquities, which was previously owned by the Jehol and Shenyang temporary palaces. This signifies that the NPM’s current artifact collection contains Qing court artifacts from The Palace Museum, the Jehol temporary palace, and the Shenyang temporary palace.

Banquet

17:30-21:00 - The Grand Hotel

The Grand Hotel retains the elements of classic Chinese architecture in its building. It looks out onto the winding banks of Keelung River. During nighttime banquets, the stunning view of the city lights can be priceless as all guests raise their glasses in a simultaneous toast.
Semi-Final of 2018 TTTC's E. J. McCluskey Doctoral Thesis Award

The 2017 Asian Test Symposium (ATS) doctoral thesis award is one of the semi-finals of the 2018 TTTC's E. J. McCluskey Doctoral Thesis Award. Named after Prof. E. J. McCluskey, a key contributor to the field of test technology, the TTTC's doctoral thesis award serves the purpose to promote the most impactful doctoral student work, to provide the students with the exposure to the community and the prospective employers, and to support interaction between academia and industry in the field of test technology.

For the 2018 TTTC's doctoral thesis award, semi-finals will be held (to be confirmed) at the Asian Test Symposium (ATS), the VLSI Test Symposium (VTS), the European Test Symposium (ETS), and the Latin American Test Workshop (LATW). At each semi-final, a jury will determine the winner, and the semi-final winners will compete against each other in the final, held at the 2018 International Test Conference (ITC).

TTTC's E. J. McCluskey Doctoral Thesis Award will be given to the winning student and his or her advisor.

Eligibility

• Doctoral students working on test-related topics are eligible for the award.
• An individual can only participate in the contest once in a lifetime.
• Students who graduated in 2017 or will graduate in 2018 are invited.
• Participation is encouraged when the thesis is close to completion.
• Submissions to multiple regional sites are prohibited.
GSC Hiroshima High School Student Research Poster Presentation 2017

- Global Science Campus is a project supported by Japan Science and Technology Agency (JST) to promote science education for high school students.
- Hiroshima University has implemented GSC Hiroshima to provide educational programs in the field of mathematics, geoscience, chemistry, physics, biological science, information and agriculture.
- GSC Hiroshima aims to foster the next generation of leaders in the areas of science and technology by developing the capacities of talented students.

<table>
<thead>
<tr>
<th>Name</th>
<th>Title of presentation</th>
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<tbody>
<tr>
<td>Sotaro SUZUKI</td>
<td>Eco-friendly material “Alginate film”</td>
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<tr>
<td>Ryosuke NEG1</td>
<td>Development of a device to detect the cerebral stroke</td>
</tr>
<tr>
<td>Yusuke TAKATO</td>
<td>Can I guess what you’re feeling right now?</td>
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<tr>
<td>Mio ITO</td>
<td>How can we sterilize bacteria efficiently using ultraviolet rays?</td>
</tr>
<tr>
<td>Futoshi EBA</td>
<td>“Discussion on radiation cooling and atmospheric pollution derived from meteorological information taken at Higashi-Hiroshima Observatory in 2011-17”</td>
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<tr>
<td>Keita KURIHARA</td>
<td>Milk-clotting enzyme derived from plants growing in Onomichi city.</td>
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<tr>
<td>Ami OCHINO</td>
<td>The Effects of Microgravity on Germination and Growth of the Plant</td>
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<tr>
<td>Hiroaki MATSUOKA</td>
<td>The point where the heights of two towers look the same</td>
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<tr>
<td>Ayaka OHUCHI</td>
<td>Does the organic chemical adsorption of MP change with different conditions</td>
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<tr>
<td>Hana KITANISHI</td>
<td>How can we increase the range of radio wave?</td>
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<tr>
<td>Riho FUKUNAGA</td>
<td>A process of the quantification of sulfur component in limestone</td>
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<td>Hikari OYO</td>
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<tr>
<td>Hinako KUNIMITSU</td>
<td>The processing method for efficient human intake of polyphenol</td>
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